Ion-Implanted High Microwave Power Indium Phosphide Transistors

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Abstract—**Indium phosphide (InP) metal–insulator–semiconductor field-effect transistors (MISFET's) have demonstrated substantially higher output power density at microwave frequencies compared to gallium arsenide metal–semiconductor field-effect transistors (MESFET's). Presented here are the microwave characteristics from an investigation of encapsulated rapid thermal annealing (RTA) for the fabrication of InP power MISFET's with ion-implanted source, drain, and active channel regions. The MISFET's had a gate length of 1.4 μm. They were made with individual gate finger widths of 100 or 125 μm, and six to ten gate fingers per device were used to make MISFET's with total gate widths of 0.75, 0.8, or 1 mm. The source and drain contact regions and the channel region of the MISFET's were fabricated using silicon implants in semi-insulating InP at energies from 60 to 360 keV with doses from 1×10^{12} to 5.6×10^{14} cm^{-2}. The implants were activated using RTA at 700°C for 30 s in N_2 or H_2 ambients using a silicon nitride encapsulant. The channel region was chemically recessed prior to depositing approximately 1000 Å of SiO_2 for the gate insulator. The high power and high efficiency InP MISFET's were characterized at 9.7 GHz, and the output microwave power density for the RTA conditions used was as high as 2.4 W/mm. For a 1 W input at 9.7 GHz gains up to 3.7 dB were observed, with an associated power-added efficiency of 29 percent. The output power density achieved was 70 percent greater than has been achieved with GaAs MESFET's.**

I. INTRODUCTION

THE INTEREST in indium phosphide (InP) metal–insulator–semiconductor field effect transistors (MISFET's) comes from several properties. InP has higher electron peak and saturation velocities than gallium arsenide (GaAs), which should provide improved operation at higher frequencies. InP also has two properties which are beneficial for high-power applications: It has a 36 percent higher breakdown field and lower ionization coefficients compared to GaAs and a 55 percent higher room temperature thermal conductivity compared to GaAs [1]. With the insulated gate, the MISFET gives considerably lower gate leakage current than the metal–semiconductor field-effect transistor (MESFET) and enables much larger positive voltages to be applied to the gate electrode. Most importantly, InP MISFET's have demonstrated substantially higher output power density and power-added efficiency compared to GaAs MESFET's [2], [3]. The insulated gate of InP MISFET's also provides higher input impedance, which eases the design of matching circuits for large-gate-width devices in monolithic microwave integrated circuit (MMIC) applications.

InP MISFET's typically suffer from a dc drain current drift problem [4]. Fortunately, the output power at microwave frequencies has been demonstrated to be much more stable than the dc drain current [2], [3]. The stability of the InP MISFET microwave output power has been observed even for devices with a partial gate structure where the gate metal does not overlap the source and drain regions [2], [3].

A wide variety of fabrication methods has been employed for GaAs power MESFET's. However most GaAs power MESFET's have employed epitaxial layers for the active channel and the source and drain regions. Some kind of channel recess has also typically been included to increase the breakdown voltage and the output power available from the power MESFET's. InP MISFET's using epitaxial active layers and a channel recess have achieved the highest output power densities and power-added efficiencies reported at 9.7 GHz [3].

There is motivation for using ion implantation in combination with rapid thermal annealing (RTA) instead of an epitaxial process. High-quality epitaxial layers can be difficult to produce in large quantities. Ion implantation is better suited for high-volume and low-cost processes. Ion implantation in semi-insulating substrates eliminates the need for a deep mesa isolation etch and provides analog device fabrication processes which are very similar to digital integrated circuit fabrication processes [5]. Thus, ion implantation is better for monolithic integration. Rapid thermal annealing of ion-implanted semiconductors decreases the time required at high temperatures compared to conventional annealing and provides reduced redistribution of substrate species and improved electrical activation.

Presented here are the results from an investigation of RTA for the fabrication of recessed gate InP MISFET's with ion-implanted source, drain, and active channel regions. Also, dc current–voltage (I–V) characteristics and power measures at 9.7 GHz are given. The output power density, power gain, power-added efficiency, and output power as a function of input power are reported.

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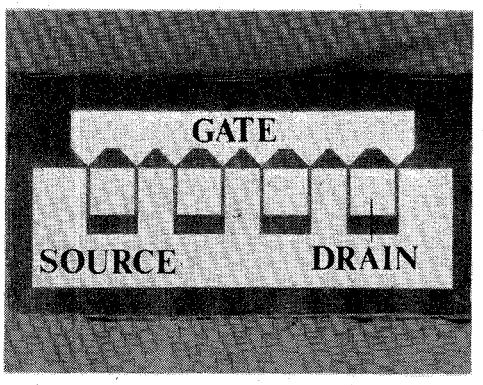

Fig. 1. Photograph of fabricated InP power MISFET with a 1 mm total gate width.

II. Experimental

The InP MISFET's investigated had a gate length of 1.4 μm. They were made with individual gate finger widths of 100 or 125 μm. The width of the individual gate fingers was limited to the above values to avoid the gain degradation that may occur at larger gate widths [6]. The InP MISFET's had six to ten gate fingers per device to produce total gate widths of 0.75, 0.8, or 1 mm. The average separation between the gate fingers was 114 μm. Large spacings were used between the gate fingers to allow enough room to make wire bonds to the individual drain regions. The spacing between the source and drain implants was 4.5 μm. The source-to-drain spacing used is similar to values used for GaAs MESFET's to provide good breakdown voltages and high reliability [7]. The length of the recessed region was 3 μm. The channel region was recessed to a thickness of approximately 0.2 μm to reduce the saturation current density to about 400 mA/mm. The total area of the largest device was 0.5 mm$\times$1.4 mm. Fig. 1 shows a micrograph of a fabricated 1 mm gate width InP MISFET.

The InP substrates used in this investigation were all 2-in-diameter wafers polished on one side with (100) crystal orientation. The wafers were grown by the liquid encapsulated Czochralski method and were iron doped with a resistivity of at least 1×10^7 $\Omega\cdot$cm. For the initial cleaning of the InP wafers a $(1:1:4)12:1$ $(HCl:HF:H_2O):H_2O_2$ solution was used for 30 s followed by a solution of 10 percent H_3PO_4 in deionized H_2O. A solution of 10 weight percent (wt %) HIO_3 in deionized H_2 was also used for 3 min. The first two solutions were also used after the HIO_3 for 15 s each. Additional details of the InP initial cleaning procedure have been previously described by Valco, Kapoor, Biedenbender, *et al.* and will not be repeated here [8], [9].

Fig. 2 illustrates cross sections of the fabrication sequence for the InP MISFET's. Step A of Fig. 2 shows photolithography for the source and drain region implants. Multiple implants were used to achieve a uniform predicted silicon concentration of 2×10^{19} cm^{-3} to a depth greater than 0.4 μm according to LSS statistics. The implants used were 6.0×10^{13}, 3.9×10^{13}, 1.7×10^{14}, 1.4×10^{14},

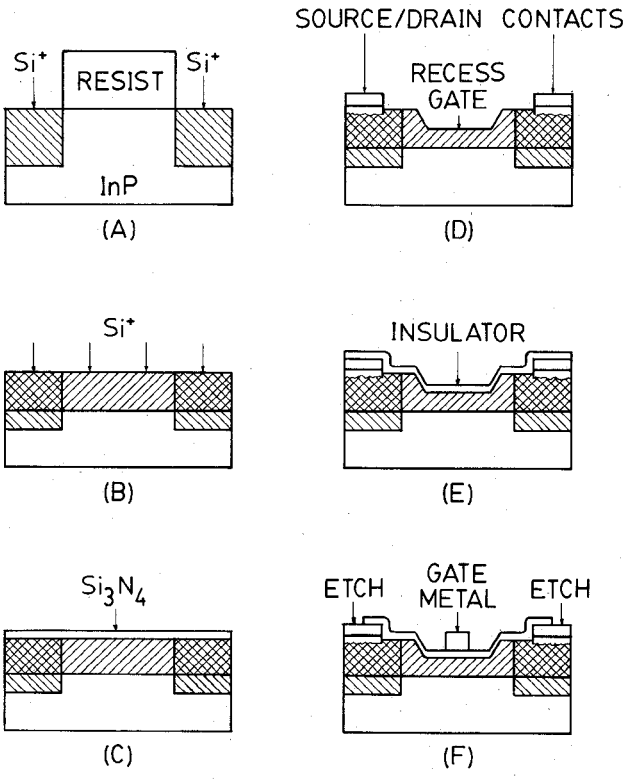

Fig. 2. Fabrication process cross sections for InP power MISFET.

and 5.6×10^{14} cm^{-2} at 40, 70, 130, 220, and 360 keV, respectively. Step B of Fig. 2 shows photolithography for the active channel region implant. Another multiple implant was used for the channel region to provide a uniform predicted silicon concentration of at least 5×10^{17} cm^{-3} to a depth of 0.4 μm. The implant schedule used was 2.5×10^{12}, 5.4×10^{12}, 1.0×10^{13}, and 1.5×10^{13} cm^{-2} at 60, 120, 220, and 360 keV, respectively. All implants were done prior to encapsulation.

Step C of Fig. 2 indicates the encapsulation of the implanted InP wafers. Silicon nitride (Si_3N_4) films with a thickness of 500 Å and a refractive index of 2.0 were used for encapsulation of the InP wafers during RTA. To remove native oxides prior to the film deposition, the InP samples were cleaned using a 1:1 H_2O:HF soak for 30 s followed by a deionized water rinse. The Si_3N_4 films were deposited on the InP wafers after implantation using a Technics Planar Etch II-A plasma reactor, operated at 13.56 MHz with automatic matching. The flow rates used during deposition were 40 sccm N_2, 40 sccm NH_3, and 9 sccm SiH_4. The deposition temperature was 300°C. The RF power used was 30 W, corresponding to a power density of 50 mW/cm^2. The details of plasma deposition on III–V compound semiconductors and corresponding silicon nitride properties have been reported by Valco and Kapoor [10], [11] and by Valco, Kapoor, Biedenbender, and Williams [12] and will not be repeated here.

After encapsulation, the InP substrates were subjected to rapid thermal annealing using a Process Products rapid heating module. Infrared lamps were used for heating. The

energy distribution of the lamps provided a broad spectrum with a peak intensity centered around a wavelength of 1 μm. All samples were slowly heated for 1–2 min to 300°C to provide uniform starting conditions before quickly ramping in approximately 10 s to 700°C. The annealing time at 700°C was 30 s. The gas flows used were 2 liters per minute of pure nitrogen or pure hydrogen. Additional details of the RTA system have been described by Biedenbender, Kapoor, and Williams and will not be repeated here [13].

Step D of Fig. 2 shows the source and drain ohmic contacts and the gate recess. The ohmic contacts consisted of a 1000 Å gold–germanium layer and 1000 Å gold overlayer alloyed at 400°C for 1 min. A second photolithography step was done after ohmic contact alloying to deposit a 5000 Å gold overlayer to assist the current handling of the devices. All metal contacts were defined by a lift-off technique. Photoresist was used to mask the gate region for the active channel gate recess. The gate region was recessed to a thickness of approximately 0.2 μm using an iodic acid solution.

Step E of Fig. 2 shows the gate insulator deposition. The gate insulator was 1000 Å of silicon dioxide deposited by indirect plasma-enhanced chemical vapor deposition. The silicon dioxide was deposited at 300°C using a mixture of silane, oxygen, and nitrogen. Additional details of the gate insulator deposition process have been described by Meiners [14].

Step F of Fig. 2 shows a gate metal for the InP MISFET's. The gate metal consisted of a 5000 Å aluminum layer and was defined using the lift-off technique. Openings were etched in the silicon dioxide gate insulator to the source and drain ohmic contact regions. The InP samples were thinned after the gate metal deposition to improve the thermal conductivity of the devices and scribed into individual MISFET's. A 500 Å titanium layer and a 5000 Å gold overlayer were deposited on the sample back side to aid the heat dissipation of the MISFET's. The completed MISFET's were packaged and wire bonded for characterization at 9.7 GHz.

III. Results

Fig. 3 shows a typical I–V characteristic for an InP power MISFET. The I–V characteristic was obtained after the drain electrodes were bonded together and was thus the total device current. The gate voltage was applied in 80 μs pulses. The extrinsic transconductance was 40 mS/mm. A drain saturation current density of 400 mA/mm for a 0 V gate bias was indicated from the I–V characteristics. The current density is comparable to the value of 376 mA/mm recently reported for ion-implanted GaAs power MESFET's [5]. According to the velocity saturation model [15], the saturation current density, I_{sat}, depends on the carrier saturation velocity, v_s, the carrier concentration, N_d, the undepleted active channel thickness, d, and the electronic charge, q, in the following manner:

$$I_{sat} = qN_d v_s d.$$

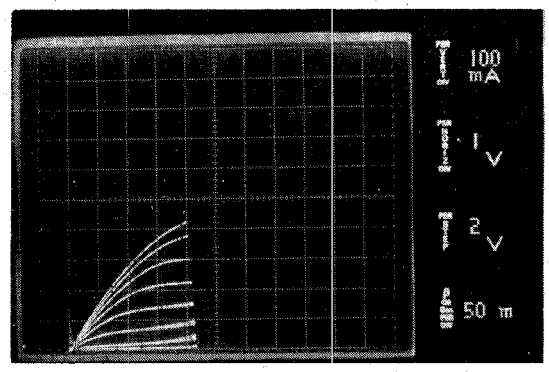

Fig. 3. I–V characteristics for a InP power MISFET with a 1 mm total gate width. The gate voltage was applied in 80 μs pulses.

However, as will be described below, the output power density for the InP MISFET's was substantially larger than the value of 0.76 W/mm obtained at 5.5 GHz for the ion-implanted GaAs MESFET's [5]. The lower output power density for the GaAs MESFET's was in part due to the bias conditions used to obtain maximum output power. To obtain maximum output power for GaAs MESFET's, the gate voltage is usually adjusted to deplete the active channel so that the drain current is one half the maximum saturation value [16]. For the drain voltage, input and output power, and power-added efficiency reported for the measurements at 5.5 GHz for the GaAs MESFET's [5], the drain current density was about 185 mA/mm. For the bias conditions used to obtain the maximum output power at 9.7 GHz from the InP MISFET's, the output current density was 309 mA/mm, as will be discussed below. Messick *et al.* [3] and Armand *et al.* [17] have previously indicated that the high drain current density in InP MISFET's, due to the high carrier saturation velocity and high product of carrier concentration and undepleted active channel thickness, was a large factor in the high output power density observed.

Fig. 4 shows output power density, power gain, and power-added efficiency as a function of drain voltage from microwave power measurements made at 9.7 GHz. The results in Fig. 4 were from a 1 mm gate width device which gave an output power density of 2.4 W/mm. The output power density achieved is 70 percent greater than has been achieved with GaAs MESFET's [18]. In Fig. 4 the output power density increased linearly with drain voltage.

The gain of the device for a 1 W microwave input was 3.7 dB with an associated power-added efficiency of 29 percent. Since the output power is at best a linear function of drain voltage, the gain in dB tends to saturate as a function of drain voltage as indicated in Fig. 4.

The power-added efficiency increased with drain voltage but started to saturate as seen in Fig. 4. The maximum power-added efficiency was 29 percent. If the microwave output power increases linearly with drain voltage and if the devices have high gain so that the microwave output power is much larger than the microwave input power, the power-added efficiency becomes constant with drain voltage, similar to the trend in Fig. 4. If the output power

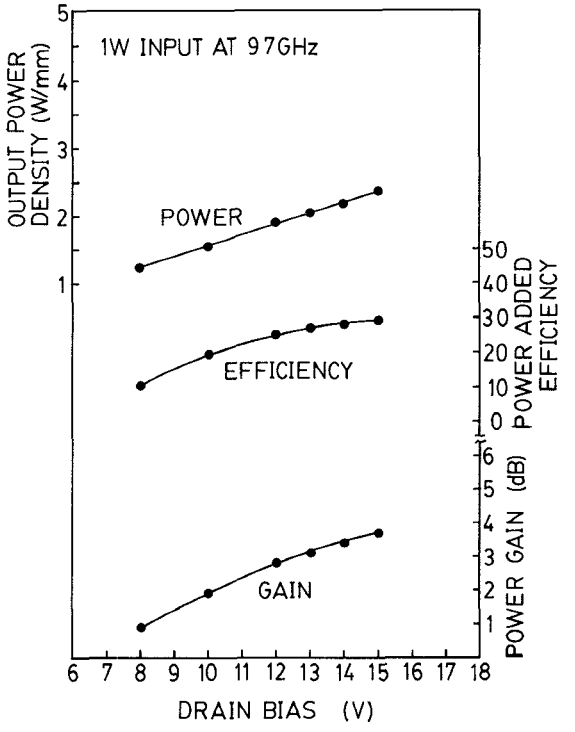

Fig. 4. Power gain, power-added efficiency, and output power density at 9.7 GHz for a InP power MISFET with a 1 mm total gate width.

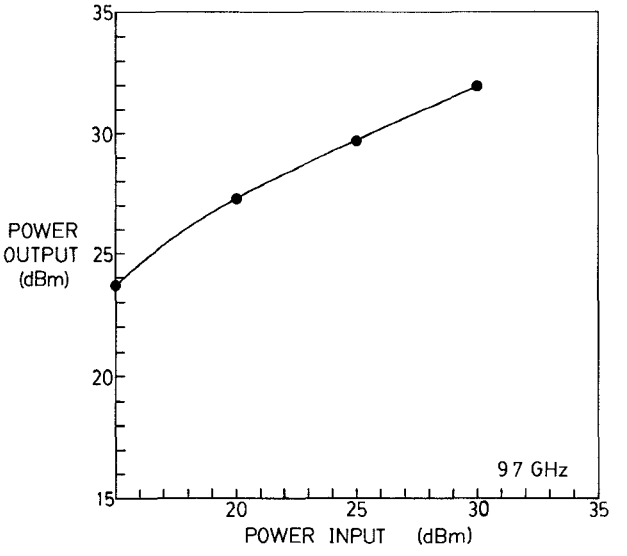

Fig. 5. Power output versus power input at 9.7 GHz for a InP power MISFET with a 0.8 mm total gate width.

density saturates as a function of drain voltage and dc power, the power-added efficiency can decrease with drain voltage, as has been observed for GaAs MESFET's [5], [6] and InP MISFET's [2], [3]. Increases in the drain voltage beyond values where the gain and power-added efficiency saturated resulted in thermal breakdown of the InP MISFET's due to the higher percentage of dc power which had to be dissipated through the device substrate.

While the above results for output power density and power-added efficiency of the ion-implanted InP MISFET's are better than have been obtained for GaAs MESFET's, they are still less than have been observed for epitaxial InP MISFET's [3]. This may be due to incomplete activation and removal of damage from the ion-implanted material. Another possible factor may be the less abrupt transition between the channel region and the semi-insulating substrate for the implanted device, which would decrease the doping concentration below the desired level for part of the channel region [2].

For the above output power density of 2.4 W/mm with an associated gain of 3.7 dB, the bias conditions were 0 V for the gate and 15 V for the drain. The above bias conditions with a 1 W input resulted in a drain current of 309 mA. The drain current decreased as the microwave input was increased, as was previously reported for epitaxial InP power MISFET's [3]. As suggested by Messick *et al.* [2], the microwave voltage at the gate terminal appears to affect the charge status of states near the semiconductor–insulator interface and causes an increasing average channel depletion width with increasing microwave input power, which results in decreasing drain current. The change in drain current with microwave input power makes measurements of input power versus output power difficult since the bias conditions used to provide high output power density with high input power cause large drain currents with lower input power, resulting in thermal breakdown.

Fig. 5 shows measurements of output power versus input power. The output powers for a 0.8 mm device were 23.7, 27.3, 29.7, and 32.0 dBm for input powers of 15, 20, 25, and 30 dBm, respectively. The corresponding gains were 8.7, 7.3, 4.7, and 2.0 dB, respectively. For GaAs MESFET's [6], [7], [16] the gain is expected to be constant at low input power and to decrease as output power saturates. For the InP MISFET's investigated here the gain decreased over a 15 dB range of input power, but for 1 mm devices high output power and useful gain were obtained for input powers of 1 W or greater. The absence of a constant gain region at low input powers may have just been a limitation resulting from how low the input power may be before thermal breakdown occurs due to high dc drain currents, as described above. It may also be possible that the gain decreases at low input powers may be related to the decrease in dc drain current with input power. As the dc drain current decreases, changes in the dc gate voltage will produce smaller dc drain current changes, and thus transconductance and gain will be lower.

IV. Summary

Rapid thermal annealing was investigated for the fabrication of microwave power InP MISFET's with ion-implanted source, drain, and active channel regions. An encapsulated process was used in which silicon nitride protected the InP substrates during rapid thermal annealing at 700°C in nitrogen or hydrogen ambients.

Pulsed I–V measurements of the InP MISFET's indicated drain saturation currents of 400 mA/mm for gate voltages of zero. The drain current decreased to 309 mA/mm when 1 W of microwave power at 9.7 GHz was

applied to the gate input. Accumulation characteristics with dc gate voltages greater than zero were not measured.

Microwave power measurements at 9.7 GHz for devices with gate widths of 0.75, 0.8, and 1.0 mm indicated output power densities as high as 2.4 W/mm. The gain for a 1 W microwave input was 3.7 dB with an associated power-added efficiency of 29 percent.

The output powers for a 0.8 mm device were 23.7, 27.3, 29.7, and 32.0 dBm for input powers of 15, 20, 25, and 30 dBm, respectively. The corresponding gains were 8.7, 7.3, 4.7, and 2.0 dB, respectively. The output power stability has been previously reported [2], [3].

The results demonstrate the superior output power density available from InP power MISFET's compared to GaAs MESFET's, and illustrate the potential of InP MISFET's for microwave and millimeter-wave power amplification.

The dc drain current drift, microwave power stability, decrease in drain current with input power, and nonconstant gain at low input power are all properties that may be affected by the quality of the gate insulator and the insulator–InP interface. Different gate insulators such as those using a phosphorus oxide [19] or a silicon interfacial region have also been shown to reduce the dc drain current drift and may also affect the above microwave properties, and are being investigated further. In addition, gate insulators that can withstand the temperatures necessary for the rapid thermal annealing of ion implants have been demonstrated [19]. These would enable self-aligned gate processes to be used, which in turn would provide full gate structures which are more stable than partial gate structures.

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REFERENCES

[1] W. Nakwaski, "Thermal conductivity of binary, ternary, and quaternary III–V compounds," *J. Appl. Phys.*, vol. 64, pp. 159–166, July 1988.

[2] L. Messick, R. Nguyen, and D. A. Collins, "Planar fully ion-implanted high power InP MISFET's," in *Proc. IEEE/Cornell Conf. Advanced Concepts in High Speed Semiconductor Devices and Circuits* (Ithaca, NY), Aug. 1987, pp. 167–176.

[3] L. Messick, D. A. Collins, R. Nguyen, A. R. Clawson, and G. E. McWilliams, "High-power high-efficiency stable indium phosphide MISFET's," in *IEDM Tech. Dig.*, 1986, pp. 767–770.

[4] J. F. Wager, S. J. T. Owen, and S. J. Prasad, "InP MISFET Technology: Interface considerations," *J. Electrochem. Soc.*, vol. 134, pp. 160–165, Jan. 1987.

[5] A. E. Geissberger, I. J. Bohl, E. L. Griffin, and R. A. Sadler, "A new refractory self-aligned gate technology for GaAs microwave power FET's and MMIC's," *IEEE Trans. Electron Devices*, vol. 35, pp. 615–622, May 1988.

[6] F. Hasegawa, "Power GaAs FETs," in *GaAs FET Principles and Technology*, J. V. DiLorenzo, Ed. Dedham, MA: Artech House, 1982.

[7] H. M. Macksey, "GaAs power FET design," in *GaAs FET Principles and Technology*, J. V. DiLorenzo, Ed. Dedham, MA: Artech House, 1982.

[8] G. J. Valco, V. J. Kapoor, and M. D. Biedenbender, "Plasma deposited silicon nitride for indium phosphide encapsulation," *J. Electrochem. Soc.*, pp. 175–182, Jan. 1989.

[9] G. J. Valco, M. D. Biedenbender, G. A. Johnson, V. J. Kapoor, and W. D. Williams, "Encapsulated annealing of InP substrates," in *Dielectric Films on Compound Semiconductors*, Proceedings of the Electrochemical Society (Pennington, NJ), vol. 86-3, pp. 209–219, 1986.

[10] G. J. Valco and V. J. Kapoor, "Role of GaAs surface cleaning in plasma deposition of silicon nitride films for encapsulated annealing," *J. Vac. Sci. Technol.*, vol. 3, pp. 873–876, July/Aug. 1985.

[11] G. J. Valco and V. J. Kapoor, "Plasma deposited silicon nitride for gallium arsenide encapsulation," *J. Electrochem. Soc.*, vol. 134, pp. 685–692, Mar. 1987.

[12] M. D. Biedenbender, V. J. Kapoor, D. Xu, and W. D. Williams, "Rapid thermal annealing of ion implanted indium phosphide," in *Dielectric Films on Compound Semiconductors*, Proceedings of the Electrochemical Society (Pennington, NJ), vol. 88-15, pp. 209–226, 1988.

[13] M. D. Biedenbender, V. J. Kapoor, and W. D. Williams, "Rapid thermal annealing of indium phosphide compound semiconductors," *J. Vac. Sci. Technol.*, vol. 5, pp. 1437–1441, July/Aug. 1987.

[14] L. G. Meiners, "Indirect plasma deposition of silicon dioxide," *J. Vac. Sci. Technol.*, vol. 21, pp. 655–658, July/Aug. 1982.

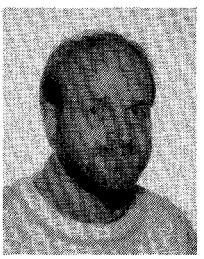
[15] M. Shur, *GaAs Devices and Circuits*. New York: Plenum Press, 1987.

[16] W. C. Niehaus, "GaAs power FETs device design principles, fabrication processes and material technology," in *GaAs FET Principles and Technology*, J. V. DiLorenzo, Ed. Dedham, MA: Artech House, 1982.

[17] M. Armand, J. Chevrier, and N. T. Linh, "Microwave power amplification with InP FETs," *Electron. Lett.*, vol. 16, pp. 906–907, Nov. 1980.

[18] H. M. Macksey and F. H. Doerbeck, "GaAs FETs having high output power per unit gate width," *IEEE Electron Device Lett.*, vol. 2, pp. 147–148, 1981.

[19] P. G. Young and V. J. Kapoor, "Silicon nitride and silicon dioxide films for MISFETs on indium phosphide," in *Dielectric Films on Compound Semiconductors*, Proceedings of this Electrochemical Society (Pennington, NJ), vol. 88-15, pp. 151–179, 1988.



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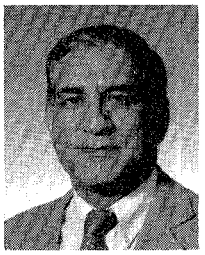

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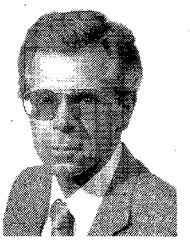

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